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Docket No. 108066-00018

Date: November 16, 2000

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a nonprovisional patent application:

For (Title): CLOCK SWITCHING CIRCUIT FOR A HOT PLUG

By (Inventors): Masato MITSUHASHI, (Kawasaki, Japan) and Yoshiyuki SHIRAI (Kawasaki, Japan).

- ☒ 24 pages of Specification/Claims 1-4/Abstract are attached.
- ☒ Formal drawings (Fig. 1-9; 9 sheets is attached.
- ☒ A Declaration and Power of Attorney is attached.
- ☒ An assignment of the invention to FUJITSU LIMITED is attached, along with Form PTO-1595 and a check for $40.00.
- ☐ An Information Disclosure Statement is attached, along with Form PTO-1449, and _____ reference(s).
- ☐ A Statement to establish small entity status under 37 C.F.R. §§1.9 and 1.27 is attached.
- ☐ A Preliminary Amendment is attached.
- ☐ Please amend the specification by inserting before the first line the sentence --This nonprovisional application claims the benefit of U.S. Provisional Application No. _____, filed _____. - -
- ☒ Priority of foreign application No. 2000-020904 filed January 28, 2000 in Japan is claimed under 35 U.S.C. §119.
- ☒ A certified copy of the above corresponding foreign application is attached.

The filing fee is calculated below and includes claim status after entry of any Preliminary Amendment noted above:

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	4 - 20	0
INDEP CLAIMS	1 - 3	0
☐ MULTIPLE DEPENDENT CLAIMS		

SMALL ENTITY			LARGE ENTITY	
RATE	FEE	OR	RATE	FEE
	$ 355	OR		$ 710
x 9 =	$	OR	x 18	$
x 40 =	$	OR	x 80	$
+135 =	$	OR	+270	$
TOTAL	$	OR	TOTAL	$ 710

- ☐ A check for the filing fee is not enclosed at this time.
- ☒ A check in the amount of 750.00 ($710 for the filing fee and $40 for the assignment recordation fee) is attached. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

George E. Oram,Jr
Registration No. 27,931

TITLE OF THE INVENTION

Clock Switching Circuit for a Hot Plug

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a clock switching circuit for switching the internal clock for an interface having a hot-plug function such as IEEE1394 or USB, and more particularly to a clock switching circuit that prevents the occurrence of hazards during switching, makes it possible to generate a stable clock, and prevents malfunction of the internal circuits.

Related Art

Recent personal computers perform the connection with peripheral devices by an interface having a hot-plug function. A hot-plug function is a function that activates the connection even when an interface cable is connected after the power to the computer and peripheral device have been turned ON. For example, when an interface cable having a hot-plug function is connected to the device to be connected after the personal computer has started up, the connection with that connected device is activated, and when the interface cable is disconnected, the connection with the connected device is deactivated.

When the connection is activated, the internal circuits of the connected device are also activated, and

specified high-speed processes, that are controlled by the synchronization clock, are executed. Moreover, after the cable has been disconnected, the connection is deactivated and the internal circuits of the connected device are also deactivated. However, internal circuits continue a minimum of operations for a preparation of the cable connection later.

The aforementioned IEEE1394 interface having a hot-plug function has a high-speed transmission rate of 400Mbps, and is a suitable interface for transmitting image data. In order to correspond with this interface, the connected device has a PLL circuit which speeds up the oscillating clock of the internal oscillator. Moreover, it is desired that while the connected device is activated, the internal circuits perform a predetermined operation in synchronization with the high-speed clock of the PLL circuit, and while the connected device is not activated, the internal circuits maintain a minimum operation in synchronization with the oscillation clock of the low-speed oscillator.

Therefore, it is necessary for the internal circuits of the connected device to switch between the high-speed clock and the low-speed clock in response to the connection or disconnection of the interface cable. In this case, it is necessary to switch between two clocks that are asynchronous and out of phase with each other. In prior clock switching circuits, it is not possible

to adequately prevent the occurrence of hazards when switching.

Fig. 1 is a circuit diagram of a prior clock switching circuit. This clock switching circuit is as disclosed in Japanese Laid-open Patent No. H01-6209309, and is used for switching asynchronous clocks in communication devices. With the switching circuit in Fig. 1, switching is performed by a selection signal 'Select' that selects between the output clock X'tal of a quartz oscillator or the output clock PLL of a PLL circuit. In order to prevent hazards, which are the cause of malfunction when switching between the asynchronous clocks X'tal and PLL, the quartz oscillator clock side comprises flip-flops F/F(1), F/F(2) and an AND gate AND1, and switching is performed in synchronization with the clock X'tal, while the PLL side also comprises flip-flops F/F(3), F/F(4) and an AND gate AND2, and switching is performed in synchronization with the clock PLL.

Fig. 2 is a timing chart of the operation of the clock switching circuit shown in Fig. 1. The selection signal 'Select' is HI-level when the interface cable is disconnected, and is LO-level when the interface cable is connected. Fig. 2 shows the operation when the interface cable changes from being connected to being disconnected, as well as the operation when returning to the connected state.

As shown in Fig. 2, when the selection signal 'Select'

is in the LO-level connection state, the clock output COUT of the switching circuit outputs the high-speed clock PLL of the PLL circuit. At that point, when the cable is disconnected and the selection signal 'Select' becomes HI-level, then in response to the fall of the clock X'tal at time t1, the flip-flop F/F(1) receives the HI-level of the selection signal 'Select'. Then, at time t2, in response to the fall of the clock PLL, the flip-flops F/F(3), (4) receive the inverted signal (LO level) of the selection signal 'Select'. In this way, the AND gate AND2 prohibits the output of the clock PLL, and the clock output COUT stops. Furthermore, in response to the fall of the clock X'tal at time t3, the flip-flop F/F(2) transfers the selection signal 'Select', and the AND gate AND1 lets the clock X'tal pass. As a result, the clock output COUT is switched to the quartz oscillator clock X'tal.

In response to the selection signal 'Select' being switched as described above, the deactivated clock is disconnected by one clock operation, and the activated clock is activated by 2 clock operations, and therefore the occurrence of hazards during switching is prevented. Furthermore, the activated clock is activated in synchronization with that clock phase, so there is no occurrence of a hazard that causes malfunction.

Fig. 3 is a different operation timing chart of the clock switching circuit in Fig. 1. In this case, the

clock PLL may operate at very high-speed when compared with the clock X'tal. In this example, the frequency of the clock PLL is two times the frequency of the quartz clock X'tal. The HI level of the selection signal 'Select' is received by the flip-flops F/F(3), (4) at time t11, which prohibits output of the high-speed clock PLL, and at time t12, the HI level of the selection signal 'Select' is received by the flip-flop F/F(1), and at the trailing edge of the quartz clock X'tal at time t13, the output of the flip-flop F/F(1) is received by the next stage flip-flop F/F(2), and the AND gate AND1 is opened and the low-speed quartz clock X'tal is output to the output clock COUT.

When the interface cable is connected, the selection signal 'Select' becomes LO-level. This state is received by the flip-flop F/F(3) at time t14, and then received by the next stage flip-flop F/F(4) at the next trailing edge at time t15. However, as described above, since the quartz clock X'tal is half or less the frequency of the high-speed flip-flop PLL, at time t16 after time t15, the flip-flops F/F(1), (2) receive the LO-level selection signal 'Select' when the clock X'tal first falls, and the output of the low-speed quartz clock X'tal is prohibited. However, at the switching inside the circle in the figure, a hazard may occur in the output clock COUT.

The IEEE1394 interface operates at 400Mbps and is

a very high-speed interface, so there is a possibility that the relationship between the PLL circuit clock and the quartz clock may become as shown in Fig. 3. In that case, with the prior clock switching circuit in Fig. 1, there is a possibility that malfunction will occur in the logical circuits in the later stages to which the output clock COUT is supplied.

Furthermore, when the interface cable is connected, the clock is switched from the low-speed quartz clock to the high-speed PLL clock, however, when the PLL circuit that starts operating after switched is unstable after switching, then an unstable clock will be supplied to the later stage circuits and malfunction will occur.

SUMMARY OF THE INVENTION

The objective of this invention is to provide a clock switching circuit that is capable of properly switching asynchronous clocks having a large difference in frequency when disconnecting or connecting an interface cable with a hot-plug function.

Furthermore, another objective of this invention is to provide a clock switching circuit that is capable of, before switching the clock, waiting for the clock of the PLL circuit to become stable after connecting an interface cable with a hot-plug function.

In order to accomplish the aforementioned objectives, one aspect of the present invention is a clock switching

circuit for switching between asynchronous first clock and second clock when connecting or disconnecting an interface cable having a hot-plug function, and comprising: a first group of flip-flops for receiving an interface disconnection signal that corresponds to disconnection and connection of the interface cable in response to the first clock; and a second group of flip-flops for receiving the interface disconnection signal in response to the second clock. Furthermore, in this invention, as for the first flip-flop group, the flip-flop of the final stage thereof outputs a first selection signal through the first clock edges whose number is the stage number of the first flip-flop group, when the interface cable is disconnected; and the flip-flop of the final stage thereof outputs a first no-selection signal through one clock edge when the interface cable is connected. Also, the first clock is selected and output in response to the first selection signal, and the output of the first clock is prohibited in response to the first no-selection signal. Moreover, as for the second flip-flop group, the flip-flop of the final stage thereof outputs a second selection signal through the second clock edges whose number is the stage number of the second flip-flop group, when the interface cable is connected; and the flip-flop of the final stage thereof outputs a second no-selection signal through one clock edge when the interface cable is disconnected. The

second clock is selected and output in response to the second selection signal, and the output of the second clock is prohibited in response to the second no-selection signal. In this invention, the second flip-flop group has more stages than the first flip-flop group by an amount that corresponds to the relationship between the frequency of the first and second clocks.

With this aspect of the invention, switching to the high-speed second clock is performed by way of the second flip-flop group having more stages, so it is possible to prevent the occurrence of hazards as occurred in the example of the prior art.

In another aspect of the invention, when the interface cable is connected, operation of the PLL circuit starts in response to the interface disconnection signal, and that interface disconnection signal is received by the second flip-flop group after a set amount of time. Also, when the interface cable is disconnected, operation of the PLL circuit stops in response to the interface disconnection signal.

With this aspect of the invention, when switching to the high-speed second clock, it is possible to output the PLL output clock, that has stabilized after a set amount of time, as the second clock. Also, when the interface cable is disconnected, operation of the PLL circuit stops immediately, so it is possible to prevent needless current consumption.

In another aspect of the invention, the number of stages of the second group of flip-flops can be varied according to the external frequency setting signal. In this way, it is possible to provide a clock switching circuit that corresponds to a plurality of types of interface cables.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a prior clock switching circuit.

Fig. 2 is a timing chart of the operation of the clock switching circuit in Fig. 1.

Fig. 3 is another timing chart of the operation of the clock switching circuit in Fig. 1.

Fig. 4 is a drawing that shows the interface cable and connected device for which an embodiment of the invention is applied.

Fig. 5 is a circuit diagram of a clock switching circuit of an embodiment of the invention.

Fig. 6 is a timing chart of the operation in Fig. 5 when the interface cable changed from being connected to disconnected.

Fig. 7 is a timing chart of the operation in Fig. 5 when the interface cable changed from being disconnected to connected.

Fig. 8 is a circuit diagram of a clock switching circuit of a second embodiment of the invention.

Fig. 9 is a drawing showing the relationship between the interface cable and the connected device in a second embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the invention is explained in reference to the drawings. However, the technical scope of the invention is not limited to the embodiments described here.

Fig. 4 shows the interface cable and connected device to which the embodiments of the invention are applied. The interface cable 20 is an interface having a hot-plug function such as IEEE1394 and USB. The connected device 30 to which the interface cable 20 is connected or disconnected has a connector 32 to which the cable is connected. In addition, there is an LSI device 34 inside the connected device 30 for processing the data signals that are supplied from the interface cable 20.

This LSI device 34 comprises a pull-up resistor R for generating a disconnection signal 'Select' to indicate whether the interface cable 20 is connected or disconnected. One end of the pull-up resistor R is connected to the power supply Vcc, and the other end is connected to one pin of the cable. The signal line on the cable side that corresponds to it is connected to ground GND, and when the interface cable 20 is connected, the disconnection signal 'Select' is LO-level, and when

the interface cable 20 is disconnected, the disconnection signal 'Select' is HI-level. This disconnection signal 'Select' is supplied to the clock switching circuit 36.

There is a quartz oscillator 33 in the connected device 30 for generating a low-speed quartz clock (first clock) X'tal, and that first clock X'tal is supplied to the clock switching circuit 36 and the PLL circuit 38. The PLL circuit 38 generates a high-speed second clock PLL while activated based on the first clock X'tal.

The clock switching circuit 36 selects either the quartz clock X'tal or the PLL circuit clock PLL according to the disconnection signal 'Select' for the interface cable, and supplies it to the circuits 40, 42 in the later stage as an output clock COUT. The later stage circuits, are for example, an FIFO buffer 40 that supplies data supplied from the interface cable 20 to the later stage, and a logic circuit 42 that processes the supplied data, and these circuits operate by using the clock COUT that is supplied from the clock switching circuit 36 as the operation clock.

Fig. 5 is a circuit diagram of a clock switching circuit of an embodiment of the invention. Figs. 6 and 7 are timing charts of the operation when the interface cable changes from being connected to disconnected, and from being disconnected to connected, respectively.

The clock switching circuit 36 shown in Fig. 5 comprises a first flip-flop group 43, which selects or

does not select the low-speed quartz clock X'tal, a second flip-flop group 45, which selects or does not select the high-speed clock PLL, and a counter 44, which counts a set amount of time after the interface cable 20 is connected until the PLL circuit becomes stable. For convenience, the PLL circuit 38 is also shown in Fig. 5.

Similar to the prior art, the first flip-flop group 43 comprises a two-stage flip-flop F/F (1), (2), and there is an AND gate 12 located between the flip-flops. Furthermore, the first flip-flop group 43 comprises an AND gate AND1 which lets the first clock X'tal pass or stops according to the output S1 of the final-stage flip-flop F/F(2). The two-stage flip-flops F/F(1), (2) receive the HI-level internal disconnection signal CLKSEL in response to the trailing edge of the first clock X'tal when the interface cable is disconnected, and the final-stage flip-flop F/F(2) outputs a first selection signal (HI level) S1 in response to the next trailing edge. In response to this first selection signal S1, the AND gate AND1 lets the first clock X'tal pass.

Moreover, when the interface cable is connected, the final-stage flip-flop F/F(2) receives a LO-level internal disconnection signal CLKSEL by way of the AND gate 12, and outputs a first no-selection signal (LO-level) S1. In response to this first no-selection signal S1, the AND gate AND1 prohibits the first clock

X'tal from passing.

As described above, the first flip-flop group 43 generates the first selection signal S1 through greater number, i.g.2, of first clock edges when the interface cable is disconnected, and generates the first no-selection signal S1 through the lesser number of first clock edge when the interface cable is connected. However, this first flip-flop group 43 is not necessarily limited to two flip-flops.

A second flip-flop group 45 comprises more stages of flip-flops F/F than the first flip-flop group 43. This difference in number of stages is set according to the difference in frequencies of the first clock X'tal and the second clock PLL. In the example shown in Fig. 5, the second flip-flop group 45 comprises 2N stages of flip-flops F/F(1a)(1b) to F/F(Na)(Nb). In addition, it comprises AND gates 181 to 18N between the flip-flops, and the AND gate AND2 lets or does not let the second clock PLL pass according to the output S2 of the final-stage flip-flop F/F(Nb).

The internal disconnection signal CLKSEL is received by the flip-flop F/F(1a) by way of an inverter 15. Moreover, when the interface cable is disconnected, the inverted signal (LO level) of the internal disconnection signal CLKSEL is received by the final-stage flip-flop F/F(Nb) by way of the AND gate 18N, and by a second no-selection signal S2, the AND gate AND2 prohibits the

second clock PLL from passing. On the other hand, when the interface cable is connected, the inverted signal (HI level) of the internal disconnection signal CLKSEL is received by the first-stage flip-flop F/F(1a), and in response to the trailing edge of the clock PLL, it is transferred to the next stage respectively. Moreover, after the trailing edge of the 2Nth clock PLL, the final-stage flip-flop F/F(Nb) outputs a second selection signal S2 (HI level), and the AND gate AND2 lets the second clock PLL pass.

When the interface cable is connected, the disconnection signal 'Select' become LO level and the PLL circuit 38 is activated and the counter 44 starts counting the leading edges of the quartz clock X'tal. And after a set number, it set the output CO to HI level and sets the internal connection signal CLKSEL to HI level. At that time the PLL circuit outputs the steady high-speed second clock PLL. On the other hand, when the interface is disconnected, the disconnection signal 'Select' becomes HI level, the PLL circuit is deactivated and stops the generation of the second clock PLL. Also, the counter 44 is preset by way of a NOR gate 46, and the output CO, as well as the internal disconnection signal CLKSEL, become HI level.

As described above, when the interface cable is connected, the PLL circuit 38 becomes activated, and the counter 44 counts until the PLL circuit becomes stable.

And after it becomes stable, the internal disconnection signal CLKSEL becomes a LO-level connection state. When the interface cable is disconnected, the internal disconnection signal CLKSEL immediately become a HI-level connection state, and the PLL circuit is deactivated in response to the trailing edge of the first clock X'tal.

The operation when the interface cable changes from being connected to disconnected will be explained using Fig. 6. At time t21, the interface cable changes from being connected to disconnected. When this happens, the connection signal 'Select' changes to HI level. In response to this, the internal disconnection signal CLKSEL becomes HI level. Together with this change, the final-stage flip-flop F/F(Nb) outputs the LO-level second no-selection signal S2 in response to the trailing edge of the second clock PLL at time t22, and the AND gate AND2 prohibits output of the second clock PLL.

In response to the trailing edge of the first clock X'tal at time t23, the first-stage flip-flop F/F(1) receives the HI-level internal disconnection signal CLKSEL, and in response to the next trailing edge of the first clock at time t24, the final-stage flip-flop F/F(2) receives the internal disconnection signal CLKSEL, and the first selection signal S1 is set to HI level. When this happens, the first clock X'tal passes the AND gate AND1, and the output clock COUT outputs the first clock.

Moreover, in response to the HI-level first selection signal S1, the output of the AND gate 50 becomes HI, and the PLL circuit 38 is set to the deactivated state and stops.

Next, the operation during when the interface cable changes from being disconnected to connected will be explained using Fix. 7. When the interface cable changes to the connected state at time t31, the disconnection signal 'Select' becomes LO level. Due to this LO level, the counter 44 changes from the preset state to the count state, and then it starts to count the first clock X'tal. The leading edges of the first clock X'tal are counted and at time t32, the counter 44 outputs LO-level output CO. When this happens, the internal disconnection signal CLKSEL is set to the LO-level connection state. Also, the PLL circuit 38 is activated (no-power-down state) by the LO-level of the disconnection signal 'Select', and generation of the second clock PLL starts. In other words, the high-speed second clock PLL is generated based on the quartz clock X'tal.

When the internal connection signal CLKSEL becomes LO-level, that inverted signal is received by the first-stage flip-flop F/F(1a) in response to the trailing edge of the second clock PLL at time t33. Furthermore, in response to the trailing edge at time t34, the signal is transferred to the second-stage flip-flop (1b), in response to the trailing edge at time t36, the signal

is transferred to the final-stage flip-flop F/F(Nb), and the second selection signal S2 (HI level) is output.

Before the final-stage flip-flop output the second selection signal S2, the first-stage and second-stage flip-flops F/F(1), (2) receive the internal connection signal CLKSEL in response to the trailing edge of the first clock X'tal, and outputs the first no-selection signal S1 (LO level), and output of the first clock X'tal is prohibited. Also, after a specified dead zone, the second clock PLL passes through the AND gate AND2 at time t36, and is output as the output clock COUT.

As described above, when the interface cable is connected, the PLL circuit that was deactivated becomes activated, and when the second clock PLL, that has become stable after a set time, is output, the internal disconnection signal CLKSEL is set to the connection state (HI level). In response to this internal disconnection signal CLKSEL, first, the first flip-flop group 43 stops output of the first clock X'tal, and then the second flip-flop group 45 having larger stages than the first group 43, starts output of the high-speed second clock PLL. Therefore, switching to the stable second clock can be performed with no occurrence of hazards.

Fig. 8 is a circuit diagram of the clock switching circuit in a second embodiment of the invention. The same reference numbers are used as were used in Fig. 5. The clock switching circuit 36 in Fig. 8 is different

from the circuit shown in Fig. 5 in that the number of stages of the second flip-flop group 45 can be changed according to the frequency selection signals Freq1,2. In order to accomplish this, there is a stage-number selection circuit 52 in the clock switching circuit 36 shown in Fig. 8.

Fig. 9 shows the relationship between the interface cable and connected device in the second embodiment of the invention. In this embodiment, there is a switch 21 in the interface cable 20 that corresponds to the operating frequency of the interface. In the embodiment shown in Fig. 9, this switch is set to the top position, so the frequency selection signal Freq1 is selected. In addition, the selection circuit 52 selects a signal from the greater number of stages and supplies it to the AND gate 18N. The operation at that time is the same as for the first embodiment.

On the other hand, when the switch of the interface cable 20 is set to the lower position, the frequency selection signal Freq2 is selected, and the selection circuit 52 selects the output of the second-stage flip-flop F/F(1b) and supplies it to the AND gate 18N. The second flip-flop group 45 becomes the third-stage flop-flop, and its operation is similar to the prior art shown in Fig. 1.

In this second embodiment of the invention, it is possible to select the number of stages of the second

flip-flop group according to the difference in the frequency between the first clock X'tal and the second clock PLL, and it is possible to set the dead zone at the time of switching the clock to an optimum length.

With this invention, it is possible to switch between a low-speed clock and high-speed clock in response to disconnection or connection of an interface cable, without the occurrence of hazards. Moreover, when the interface cable is connected, switching waits for a stable high-speed clock to be generated before switching, so it is possible to prevent malfunctioning of the circuit that supplies the clock.

The protected range of this invention is not limited to the embodiments described above, but includes the invention and equivalent objects of the range disclosed in the claims.

WHAT IS CLAIMED IS:

1. A clock switching circuit that switches between asynchronous first and second clocks according to whether an interface cable, having a hot-plug function, is connected or disconnected and comprising:

a first flip-flop group that receives an interface disconnection signal that corresponds to the disconnection or connection of the interface cable in response to said first clock, wherein when the interface cable is disconnected, the final-stage flip-flop thereof outputs a first selection signal through the first clock edges whose number is the stage number of the first flip-flop group, and when said interface cable is connected, the final-stage flip-flop outputs a first no-selection signal through one first clock edge, said first flip-flop group outputting said first clock in response to said first selection signal, and prohibitting output of said first clock in response to said first no-selection signal;

a second flip-flop group that receives said interface disconnection signal in response to said second clock, wherein when said interface cable is connected, the final-stage flip-flop thereof outputs a second selection signal through the second clock edges whose number is the stage number of the second flip-flop group, and when said interface cable is disconnected, the final-stage flip-flop outputs a second no-selection signal through

one second clock edge, said second flip-flop group outputting said second clock in response to said second selection signal, and prohibiting output of said second clock in response to said second no-selection signal; and

where the number of stages of said second flip-flop group is greater than the that of said first flip-flop group according to the relationship between the frequency of said first and second clocks.

2. The clock switching circuit of claim 1 wherein;

said second clock is supplied from a PLL circuit that generates said second clock from said first clock, and

when said interface cable is connected, operation of said PLL circuit starts in response to said interface disconnection signal, and said interface disconnection signal is received by said second flip-flop group after a set time therefrom.

3. The clock switching circuit of claim 2 wherein;

when said interface cable is disconnected, operation of said PLL circuit stops in response to said interface disconnection signal.

4. The clock switching circuit of claim 1 wherein;

the number of stages of said second flip-flop group is capable of being changed according to the operating

clock frequency of said interface cable to be connected.

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ABSTRACT

One aspect of the present invention is a clock switching circuit for switching between asynchronous first clock and second clock when connecting or disconnecting an interface cable having a hot-plug function, and comprising: a first group of flip-flops for receiving an interface disconnection signal that corresponds to disconnection and connection of the interface cable in response to the first clock; and a second group of flip-flops for receiving the interface disconnection signal in response to the second clock. Furthermore, in this invention, as for the first flip-flop group, the flip-flop of the final stage thereof outputs a first selection signal through the first clock edges whose number is the stage number of the first flip-flop group, when the interface cable is disconnected; and the flip-flop of the final stage thereof outputs a first no-selection signal through one clock edge when the interface cable is connected. Also, the first clock is selected and output in response to the first selection signal, and the output of the first clock is prohibited in response to the first no-selection signal. Moreover, as for the second flip-flop group, the flip-flop of the final stage thereof outputs a second selection signal through the second clock edges whose number is the stage number of the second flip-flop group, when the interface cable is connected; and the flip-flop of the final stage

thereof outputs a second no-selection signal through one clock edge when the interface cable is disconnected. The second clock is selected and output in response to the second selection signal, and the output of the second clock is prohibited in response to the second no-selection signal. In this invention, the second flip-flop group has more stages than the first flip-flop group by an amount that corresponds to the relationship between the frequency of the first and second clocks.

Docket # 95,174

09777 "420E260

FIG. 1

Prior Art

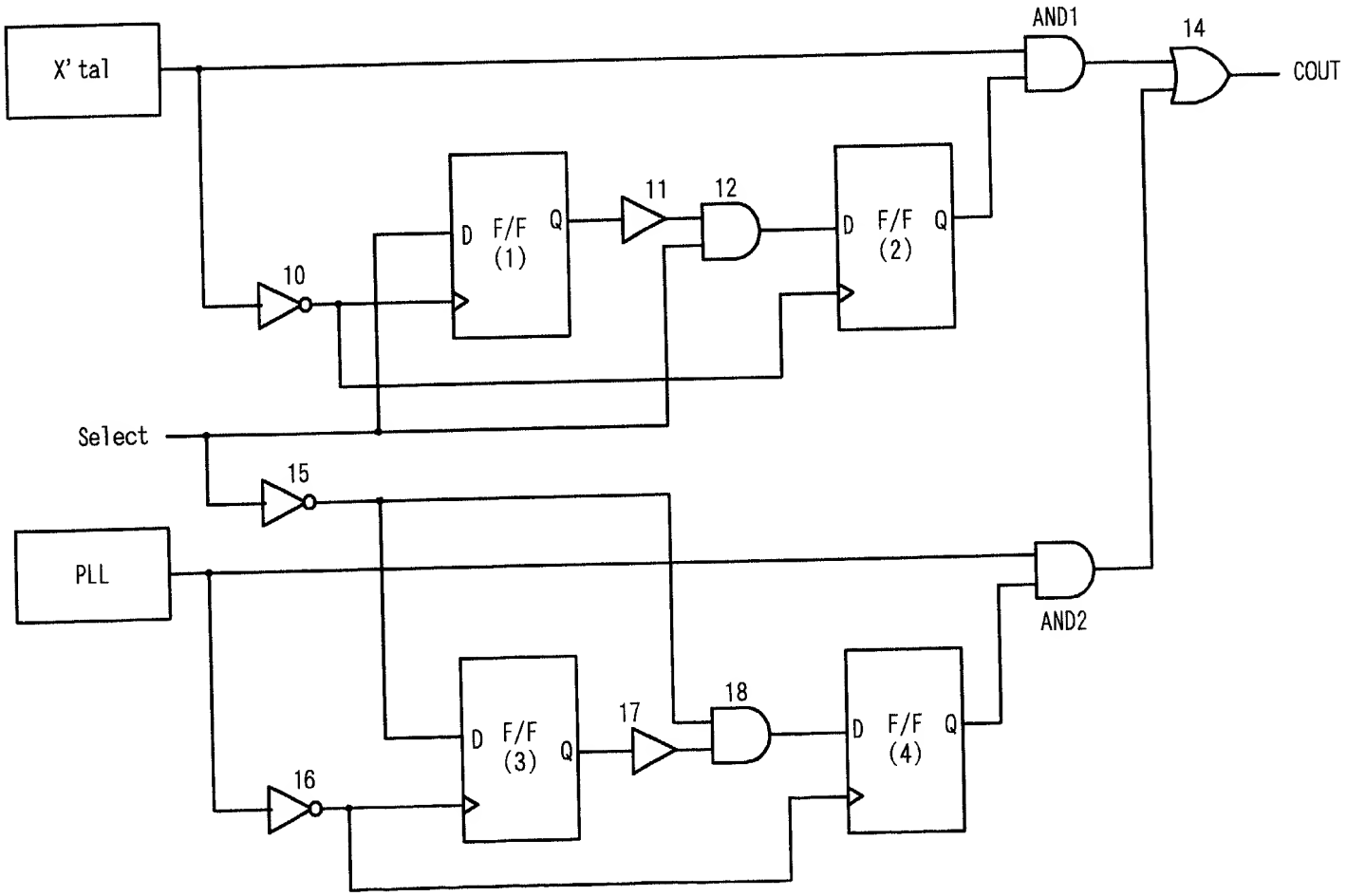


FIG. 2

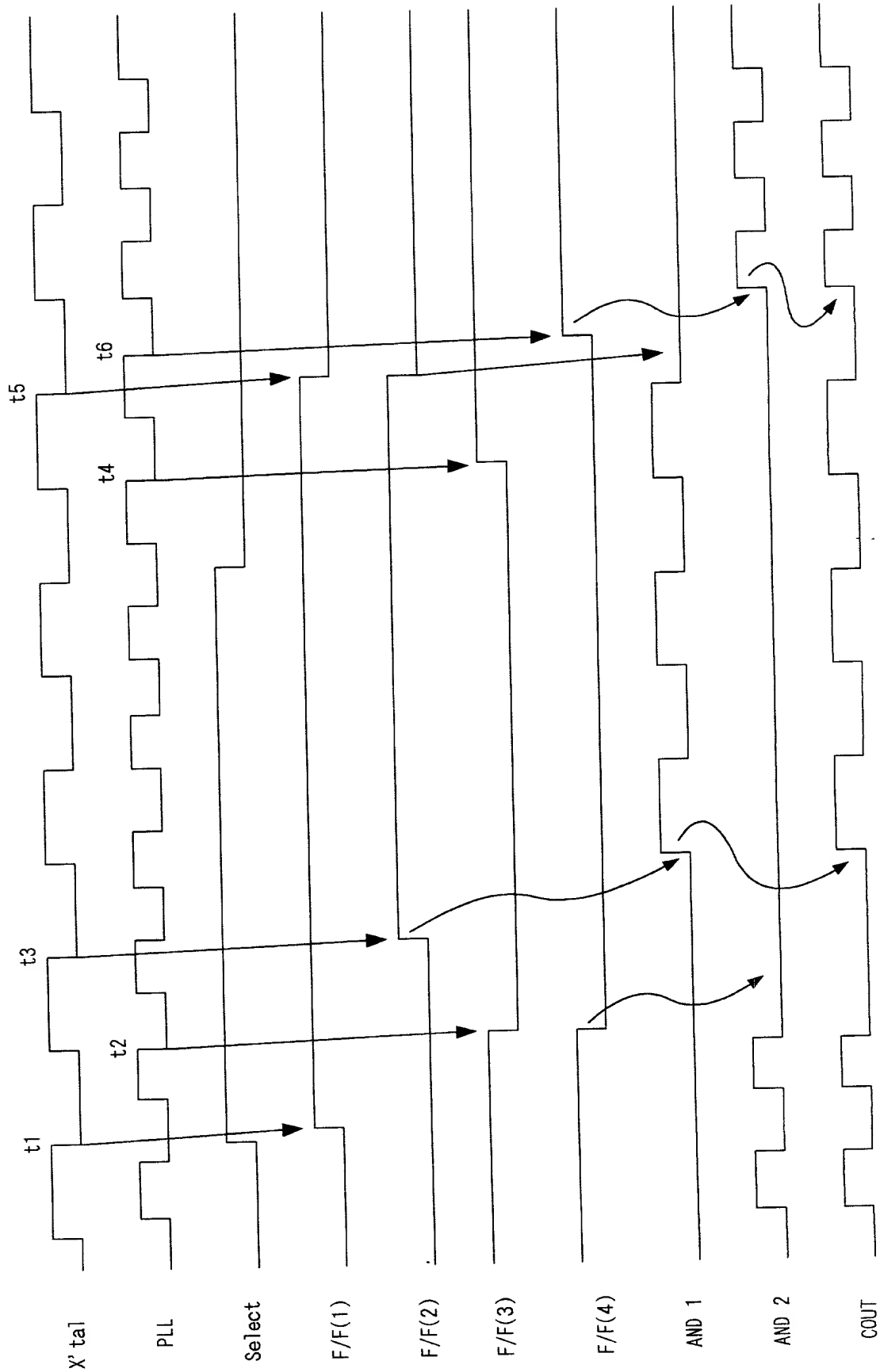
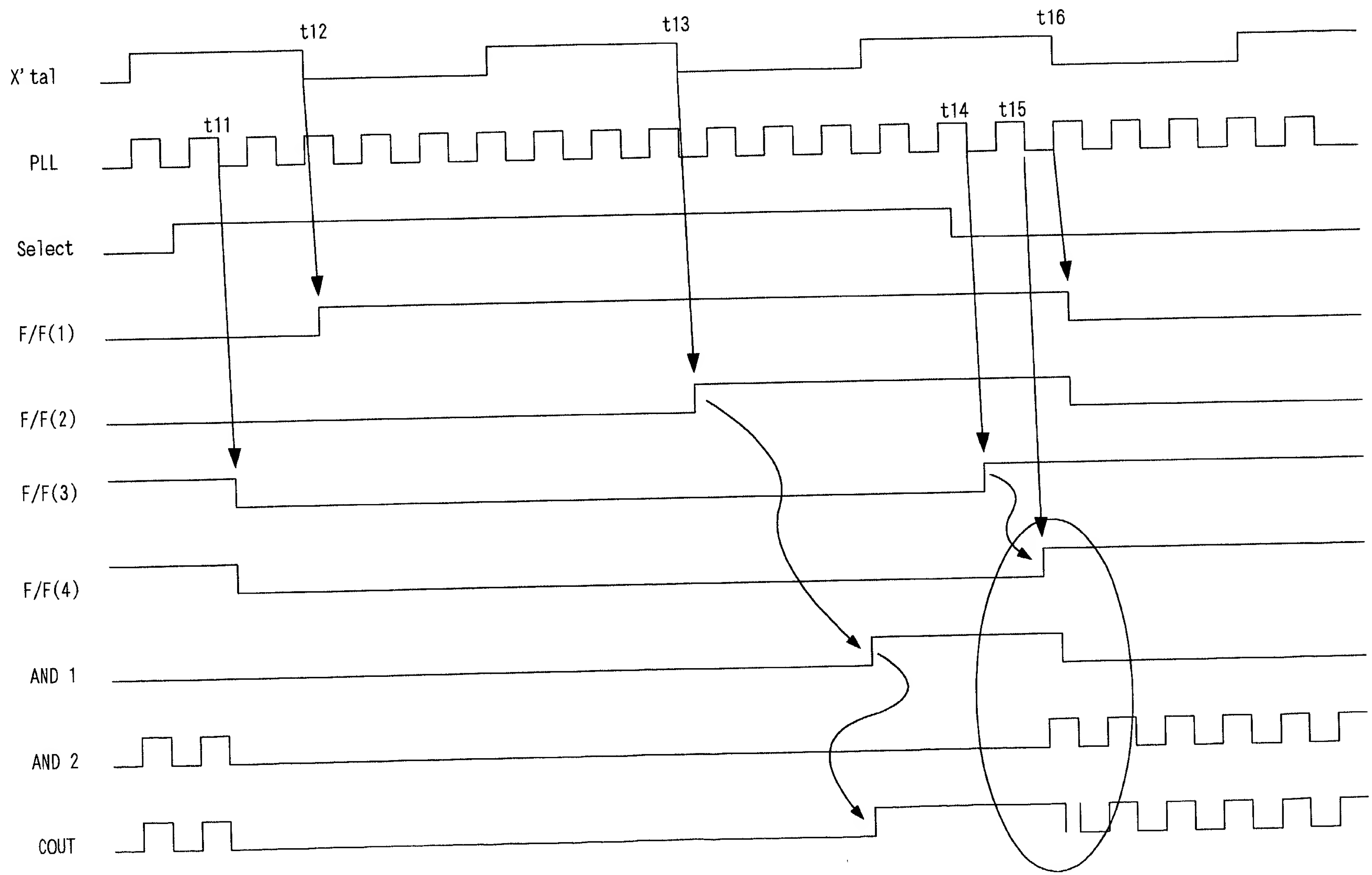
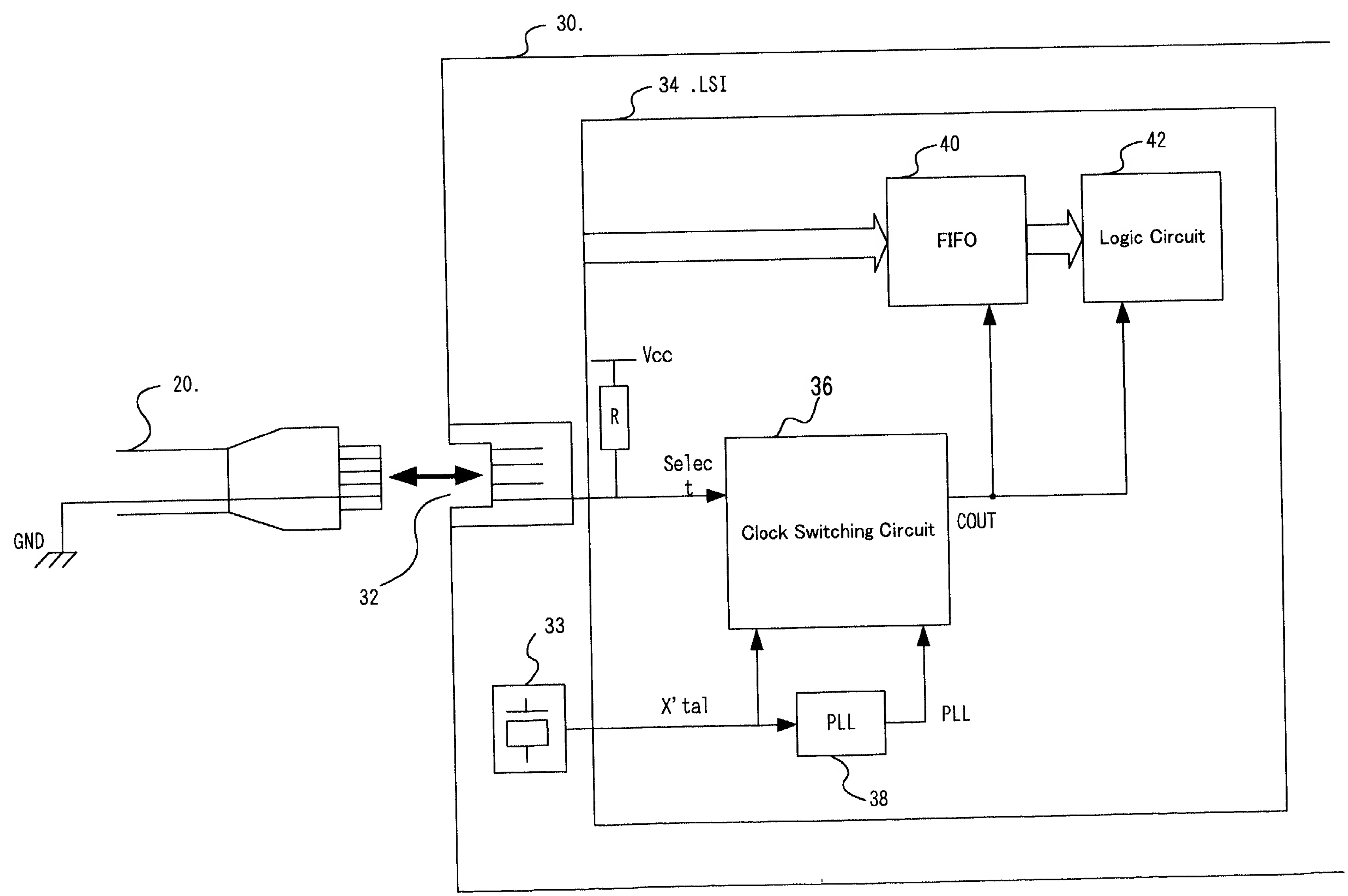


FIG. 3



X' tal
PLL
Select
F/F(1)
F/F(2)
F/F(3)
F/F(4)
AND 1
AND 2
COUT
t11
t12
t13
t14
t15
t16

FIG. 4



30.
34 .LSI
40
42
FIFO
Logic Circuit
Vcc
R
20.
36
Selec
t
Clock Switching Circuit
COUT
GND
32
33
X' tal
PLL
PLL
38

FIG. 5

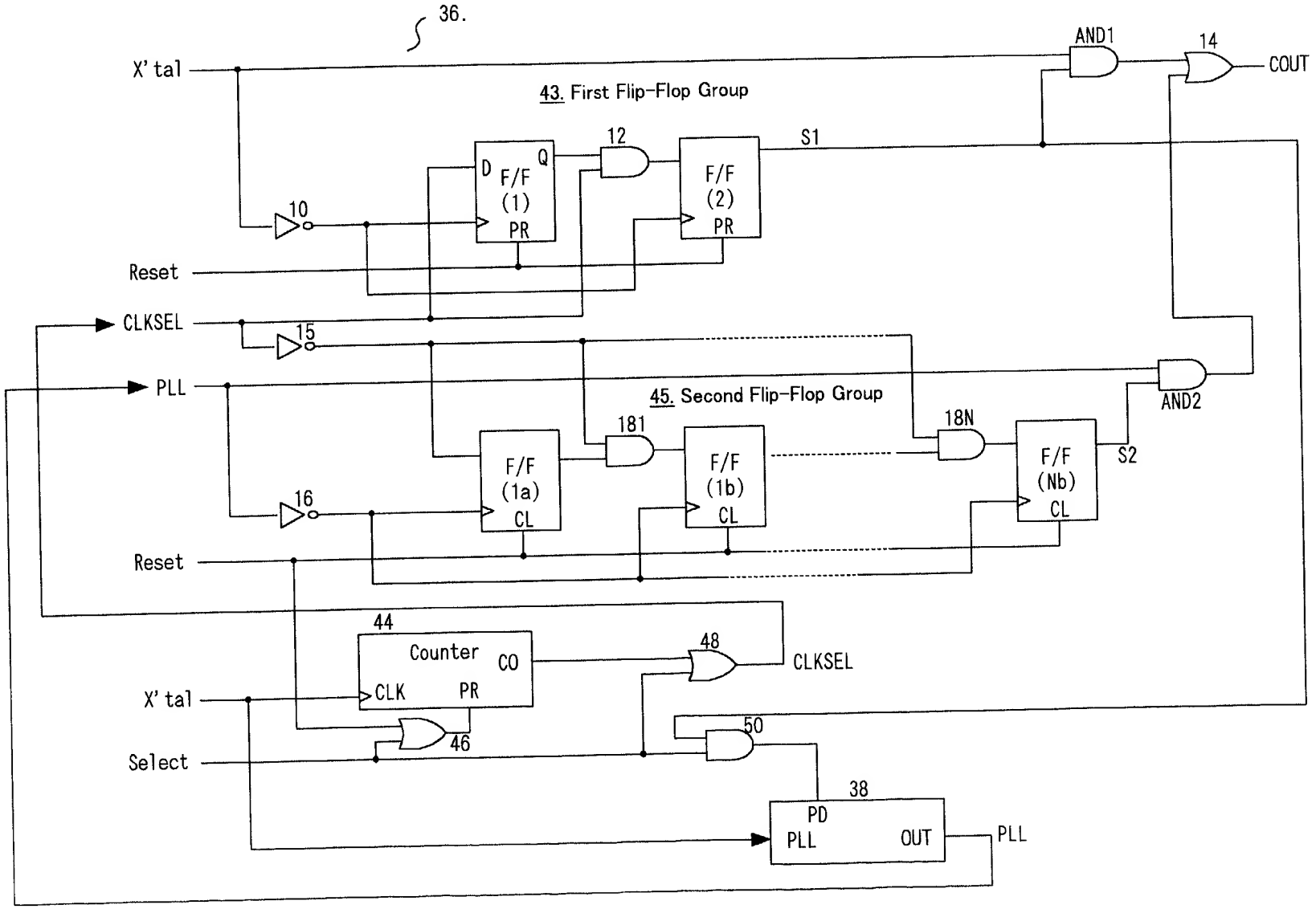
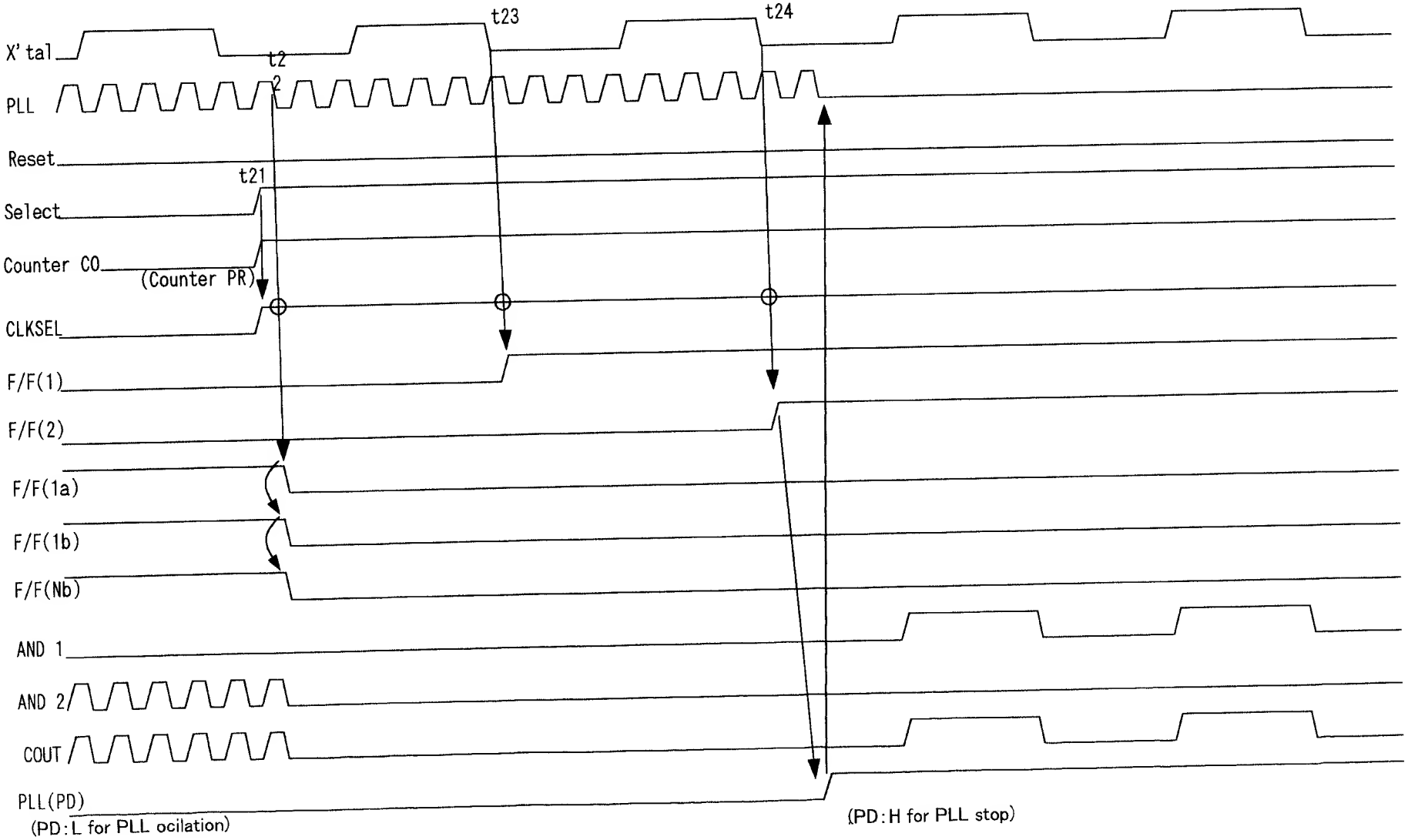

36.
X'tal
AND1
14
COUT
43. First Flip-Flop Group
12
S1
D
Q
F/F
(1)
PR
F/F
(2)
PR
10
Reset
CLKSEL
15
PLL
45. Second Flip-Flop Group
181
18N
AND2
F/F
(1a)
CL
F/F
(1b)
CL
F/F
(Nb)
CL
S2
16
Reset
44
Counter
CO
CLK
PR
48
CLKSEL
X'tal
46
50
Select
38
PD
PLL
OUT
PLL

FIG. 6

To disconnection



DOCKET NUMBER

FIG. 7

To connection

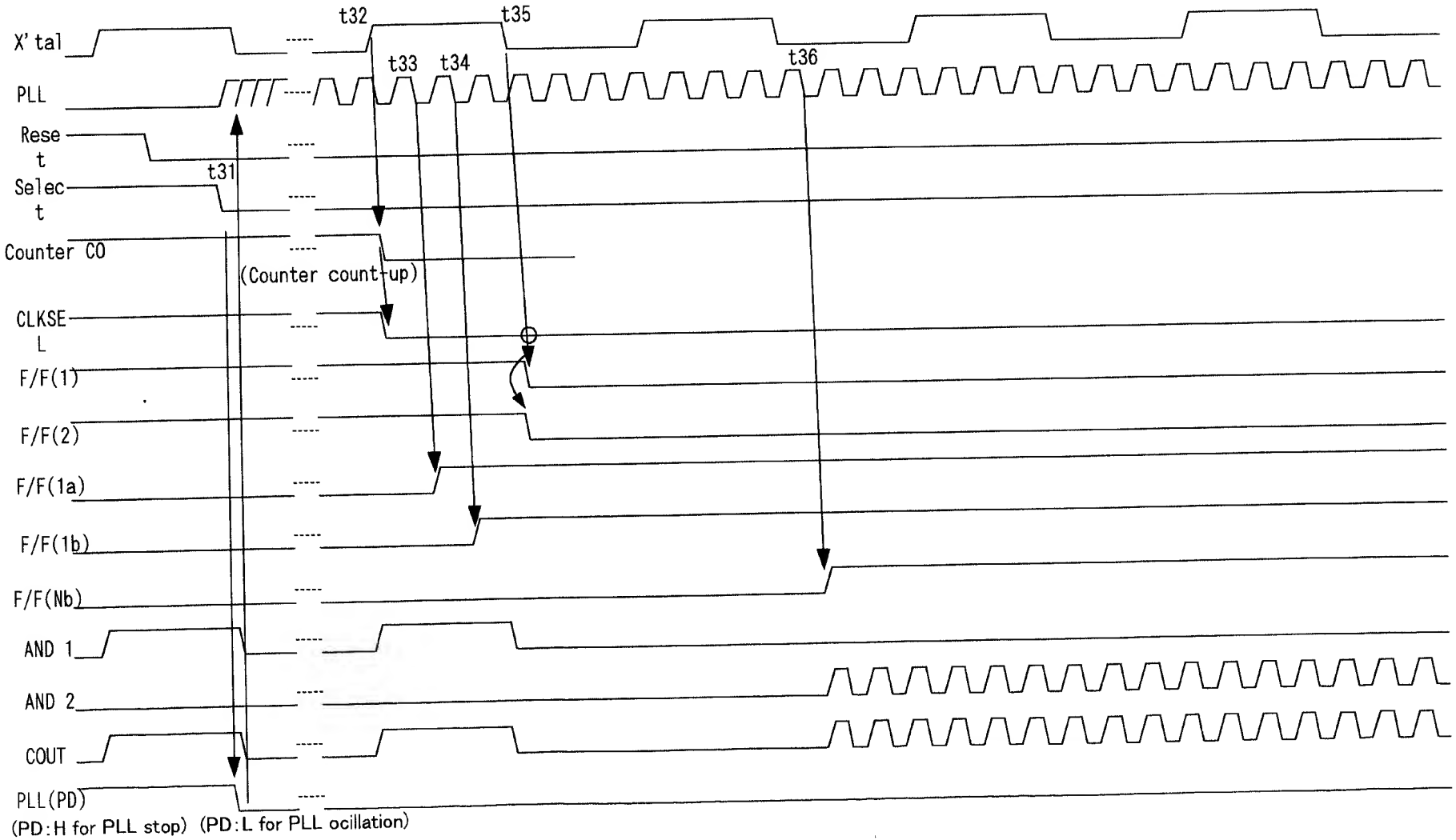


FIG. 8

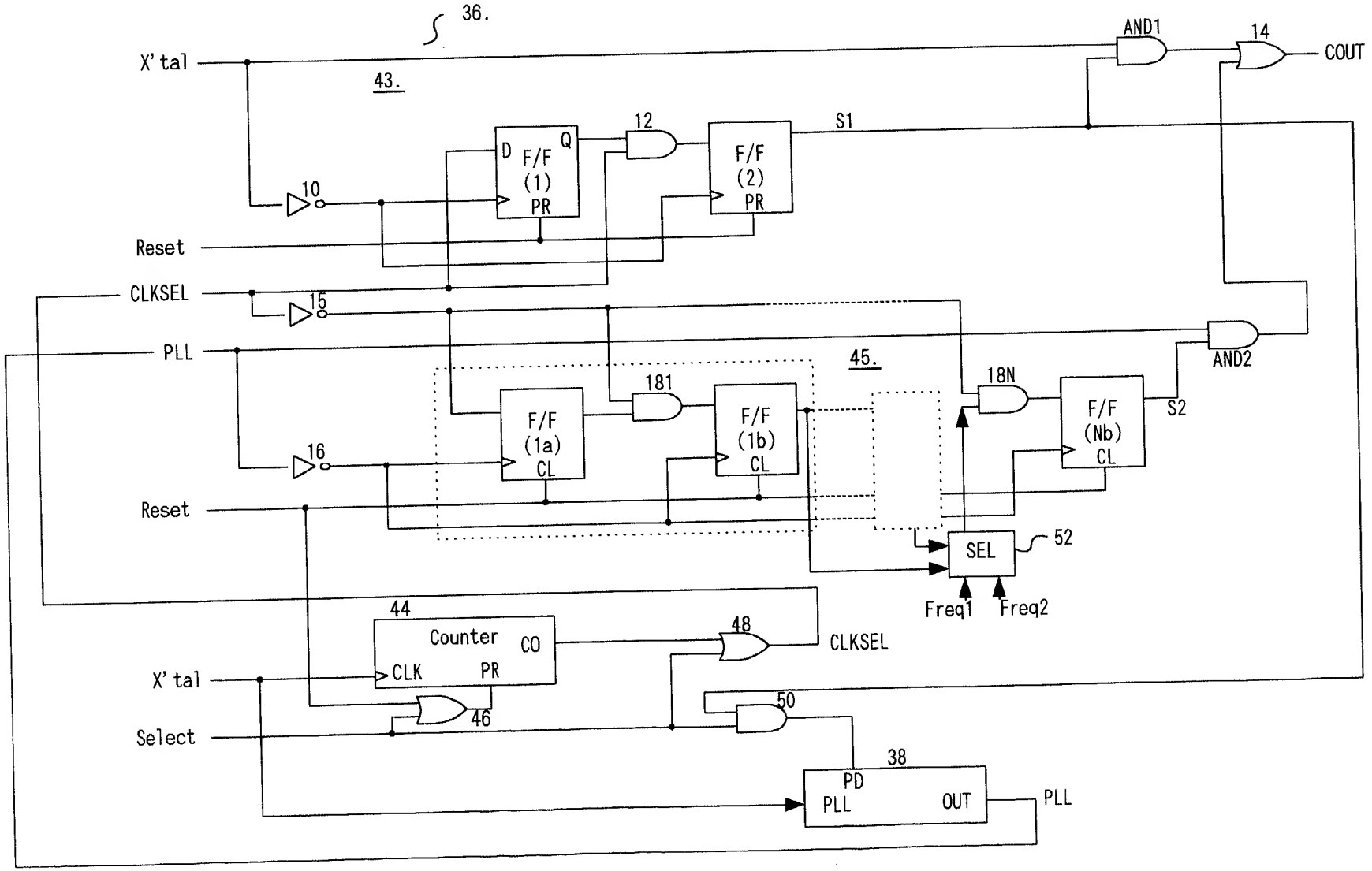
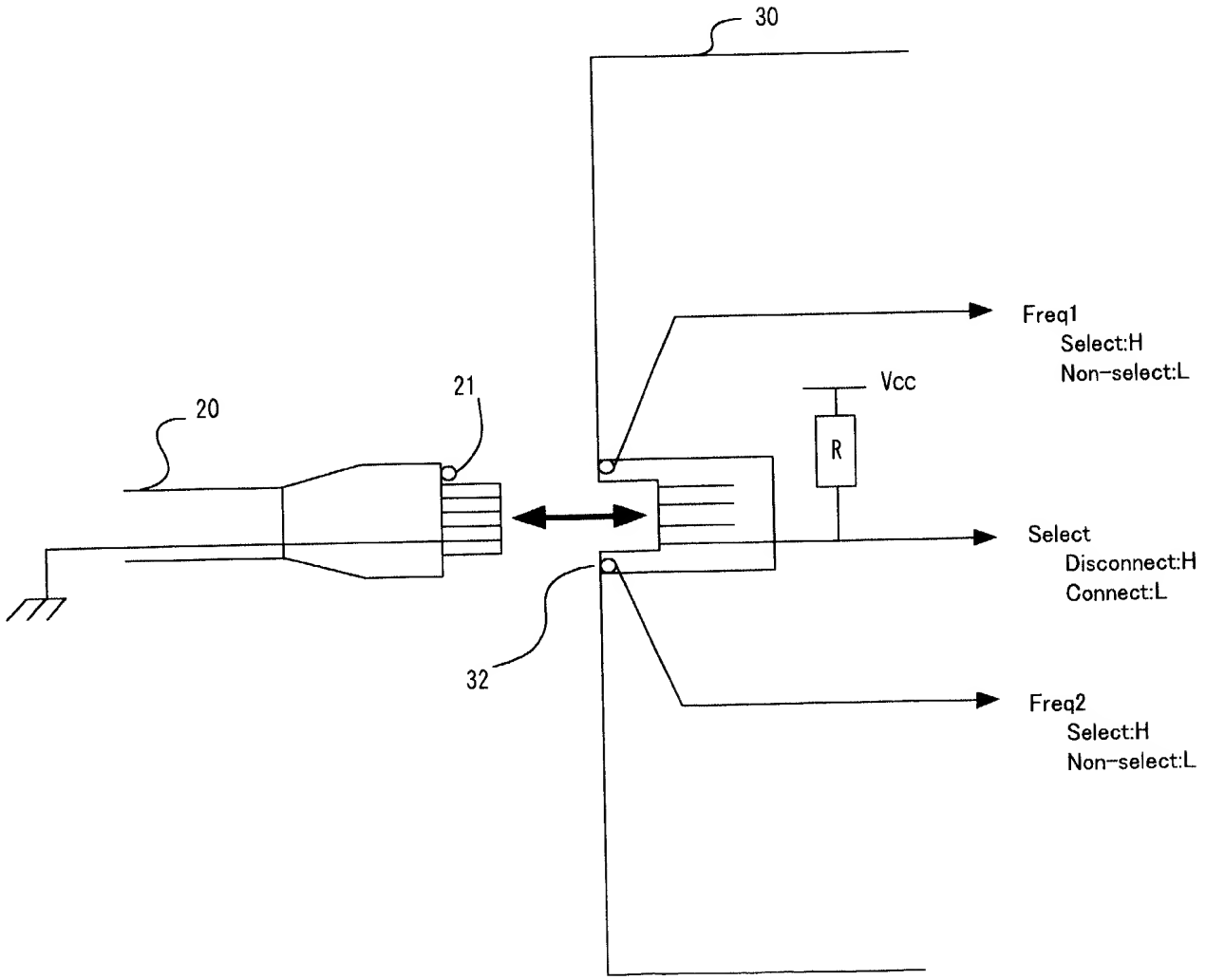

36.
X' tal
43.
AND1
14
COUT
12
S1
D
F/F
(1)
PR
Q
F/F
(2)
PR
10
Reset
CLKSEL
15
PLL
45.
AND2
181
18N
F/F
(1a)
CL
F/F
(1b)
CL
F/F
(Nb)
CL
S2
16
Reset
SEL
52
Freq1
Freq2
44
Counter
CO
CLK
PR
48
CLKSEL
X' tal
46
50
Select
38
PD
PLL
OUT
PLL

FIG. 9


30
Freq1
Select:H
Non-select:L
Vcc
R
21
20
Select
Disconnect:H
Connect:L
32
Freq2
Select:H
Non-select:L

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Declaration and Power of Attorney For Patent Application

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As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CLOCK SWITCHING CIRCUIT FOR A HOT PLUG

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the specification of which is attached hereto unless the following box is checked:

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☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

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Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
2000-20904	Japan	28/01/2000	☐
			☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

書類送付先

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Monica Chin Kitts, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; Karen K. Costantino, Reg. No. 35,107; James A. Poulos, III, Reg. No. 31,714; Patrick D. Muir, Reg. No. 37,403; Sharon N. Klesner, Reg. No. 36,335; and Murat Ozgu, Reg. No. 44,275; Bradley D. Goldizen, Reg. No. 43,637; and N. Alexander Nolte, Reg. No. 45,689.

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(Supply similar information and signature for third and subsequent joint inventors.)